CLAIMS

1. A method of calibrating a timer having a coarse measurement capability in which time intervals defined by boundaries are counted and a fine measurement capability in which time between boundaries is interpolated using a voltage ramp, comprising:

   a. Determining alignment of the voltage ramp relative to a reference-clock signal having a known relationship to the boundaries;

   b. Sampling the voltage ramp at a plurality of known times relative to the boundaries; and

   c. Determining slope of the voltage ramp as a function of time from the voltage samples.

2. The method of claim 1, further comprising aligning the voltage ramp relative to the time interval boundaries.

3. The method of claim 2, wherein the time intervals are defined by an interval clock signal at a first frequency, further comprising phase-locking the interval clock signal to a reference-clock signal at a second frequency so that phase relationship between the interval-clock signal and the reference-clock signal is defined.

4. The method of claim 3, wherein phase-locking comprises operating a phase-locked loop to maintain a defined phase relationship between the interval-clock signal and the reference-clock signal.

5. The method of claim 2, wherein aligning the voltage ramp comprises starting the voltage ramp at a defined number of periods of the reference-clock signal following coincidence of the interval-clock signal and the reference-clock signal.

6. The method of claim 2, wherein sampling the voltage ramp at a plurality of known times comprises: starting the voltage ramp following a first number of cycles of the reference-clock signal following coincidence of the interval-clock signal and the reference-clock signal, and sampling the voltage ramp at a subsequent clock edge of the interval-clock signal to obtain a first voltage sample.

7. The method of claim 6, wherein sampling the voltage ramp at a plurality of known times comprises: starting the voltage ramp following a second number of cycles of the reference-clock signal following coincidence of the interval-clock signal and the reference-clock signal; and sampling the voltage ramp at a subsequent clock edge of the interval-clock signal to obtain a second voltage sample.

8. The method of claim 7, wherein the interval-clock signal and the reference-clock signal are substantially out of phase with one another when voltage ramp is sampled.

9. The method of claim 8, further comprising determining from the phase relationship between the interval-clock signal and the reference-clock signal a time difference between the respective known times at which the voltage ramp is sampled to obtain the first voltage sample and the second voltage sample.

10. The method of claim 9, wherein determining slope of the voltage ramp comprises calculating the a ratio of difference in voltage between the second voltage sample and the first voltage sample to the time difference between the respective known times at which the voltage ramp is sampled to obtain the first voltage sample and the second voltage sample.

11. Apparatus having an event timer and comprising:

a. A coarse-measurement counter for counting time intervals defined by boundaries,

b. A fine-measurement interpolator employing a voltage ramp to measure a time delay of less than one of the time intervals;

c. A source of an interval-clock signal at a first frequency and a reference-clock signal at a second frequency with a defined phase relationship between the interval-clock signal and the reference-clock signal;

d. An analog-to-digital converter for sampling the voltage ramp at a plurality of known times relative to the boundaries to obtain voltage samples from which slope of the voltage ramp can be calculated.

12. The apparatus of claim 11, further comprising a processor for determining slope of the voltage ramp as a function of time from the voltage samples.

13. The apparatus of claim 11 wherein the source comprises a first unit for generating the interval-clock signal, a second unit for generating the reference-clock signal, and a phase-locked loop to maintain the interval clock-signal and the reference-clock signal in a defined phase relationship.

14. The apparatus of claim 13, wherein the phase-locked loop maintains the interval-clock signal and the reference-clock signal in a defined phase relationship in which the interval-clock signal and the reference-clock signal are periodically coincident, and further comprising a counter to count cycles of the reference-clock signal and to initiate the voltage ramp when a predetermined count is reached.

15. The apparatus of claim 14, wherein the analog-to-digital converter is responsive to the counter and to the interval-clock signal to sample the voltage ramp at an edge of the interval-clock occurring subsequent to initiation of the voltage ramp.

16. A PICA probe system comprising:

a. A PICA collection camera;

b. Acquisition electronics responsive to strobe pulses from the PICA collection camera representing photon-detection events for collecting data about such events, including a timing subsystem having a coarse-measurement counter for counting time intervals defined by boundaries and a fine-measurement interpolator employing a voltage ramp to measure a time delay of less than one of the time intervals; and

c. A workstation having a processor in communication with the PICA collection camera and the acquisition electronics for controlling operation and for processing data collected by the acquisition electronics.

17. The system of claim 16, further comprising a source of an interval-clock signal at a first frequency and a reference-clock signal at a second frequency with a defined phase relationship between the interval-clock signal and the reference-clock signal, and an analog-to-digital converter for sampling the voltage ramp at a plurality of known times relative to the boundaries to obtain voltage samples from which slope of the voltage ramp can be calculated.

18. The apparatus of claim 17, further comprising a phase-locked loop to maintain the interval-clock signal and the reference-clock signal in a defined phase relationship in which the interval-clock signal and the reference-clock signal are periodically coincident, and further comprising a counter to count cycles of the reference-clock signal and to initiate the voltage ramp when a predetermined count is reached.